MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

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MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400μm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters.

During the past quarter, with the completion of STIM-2B/-3B, we have shifted more focus to completing the redesign of STIM-2/-3 and to the development of the telemetry circuits that will be needed to make these probes operate wirelessly via a telemetry interface. The negative strobes needed for the original STIM-2 design have been replaced so the interface requires only 5V logic. Separate address and data latching signals are generated on-chip by holding the CLOCK and DATA lines at designated levels during the strobe, effectively providing masking capability. In 3D probe assemblies, the strobe signal is decoded in platform electronics and is gated to only the addressed probe so that the others perform no operation when they are not addressed.

A major problem with present active probes, and especially stimulating probes, is the difficulty associated with testing the devices before final bonding and use. This is particularly true of 3D arrays where it is critical to assemble only known good devices into the arrays. At present, sites must be probed individually, requiring hours to verify the operation of each probe prior to final assembly. Test modes have been added to the redesigned STIM-2/-3 probes to allow complete testing of the probes before the final release etch and after this etch but before bonding/assembly. The test modes include: input shift register test, DAC calibration, site connection test, anodic bias test, amplifier test, and site impedance test. Thus, all important aspects of the probes can be tested from the normal probe I/O connections. This applies not only to pre-assembly but also to tests performed in-vitro and in-vivo.

A new DAC design has also been developed for STIM-2/-3 that offers much improved output resistance, power-supply independence, and charge balance in the face of device threshold variations.

In developing the circuitry required for a fully-implantable wireless interface to the probes, we have previously reported the development of the power supply, clock generator, data detector, and power-on-reset circuits. During this last quarter, the timing controller and strobe generator circuits were designed and simulated. This block receives the clock and steps it down with a user selectable ratio to synchronize it with the

demodulated input data. The data is stored in a serial shift register and parity checks are performed. Strobe signals are generated to synchronize the data to STIM-2 and the clock and data is sent to the stimulating probe. We hope to have the full telemetry interface for the stimulating probes designed, integrated, and tested before the end of the year.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data that can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0µA to ±254µA with a resolution of 2µA, while STIM-2 has a range from 0 to ±127µA with a resolution of 1µA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a

multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, work has proceeded on both the development of the high-end STIM-2/-3 probes with on-chip current generation. An extensive set of self-test modes have been built into this probe to facilitate bench testing and a new DAC circuit with improved output swing has been developed. Additional circuit blocks for a fully-implantable wireless telemetry link have also been developed and will soon be fabricated. The results in each of these areas are described more fully in the sections below.

2. STIM-2/3: A Multiplexed Stimulating Probe with On-Chip Current Generation

With the completion of STIM-2B/-3B, work has focused more strongly on completing the redesign of STIM-2, our high-end multiplexed stimulating probe with on-chip current generation. In the original design of STIM-2, negative strobes were inserted into signal strings on the clock and data lines to synchronize the operation of the system. Generation of these negative strobes complicated the overall system and they have been eliminated with the addition of an additional strobe input to the probe. The new timing diagram is shown in Fig 1.

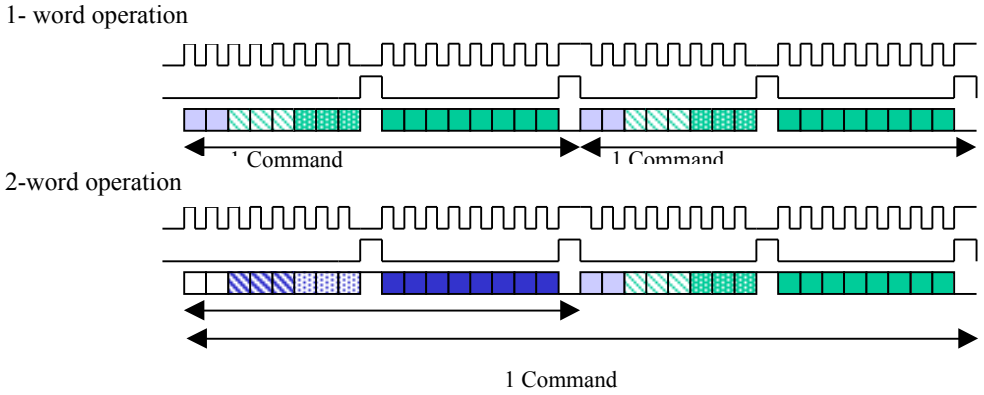


Fig. 1: New timing diagram for STIM-2

After an 8-bit data string has been clocked into the shift register, a strobe signal is detected. At this point, the CLOCK line is held low and DATA line is high so a data strobe signal is generated and the input data are latched and decoded. Then another 8-bit

data string follows in on the DATA line, and a strobe signal is again applied on the STB line. This time the CLOCK line is high and the DATA line is low so a clock strobe signal is generated and a particular operation is realized corresponding to the input mode selected. For 2-word operations, the mechanism for generating the strobe signals is the same except that the operation uses the strobe signals twice. For 3D applications, to select between different probes mounted on a common platform, the STB line is decoded in platform circuitry first and is then fed only to the selected probe as shown in Fig. 2. Unselected probes have their corresponding STB-probe signal masked. Although the data is still clocked into the shift registers of all the probes, no action is taken in the absence of the strobes.

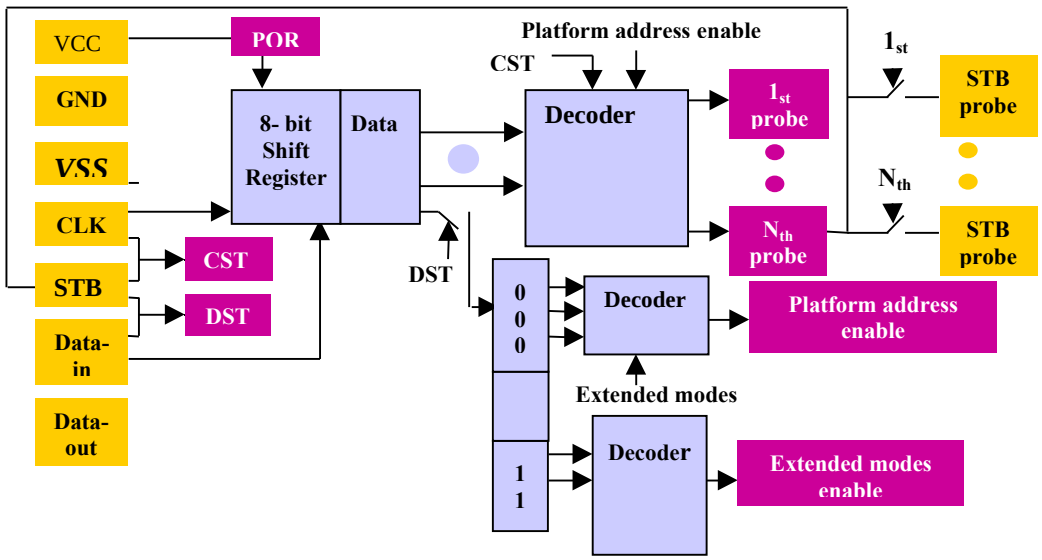


Fig. 2: Block diagram of the platform addressing circuitry. The input lines are shown at the left and the probes are shown at right. The probe address is decoded and used to multiplex the strobe to the intended device.

Test modes have been added for on-chip self-test. This is critical to allow the probes to be fully tested before assembly into acute or chronic arrays, especially for STIM-3. Figure 3 shows the new mode designations. Test modes include: shift register test, DAC calibration, site connection test, anodic bias test, amplifier test and impedance test. These modes operate with 2-word commands since they are not frequently utilized. Using an external circuit board, we can test the probes with LABVIEW automatically without laboriously probing the sites one by one.

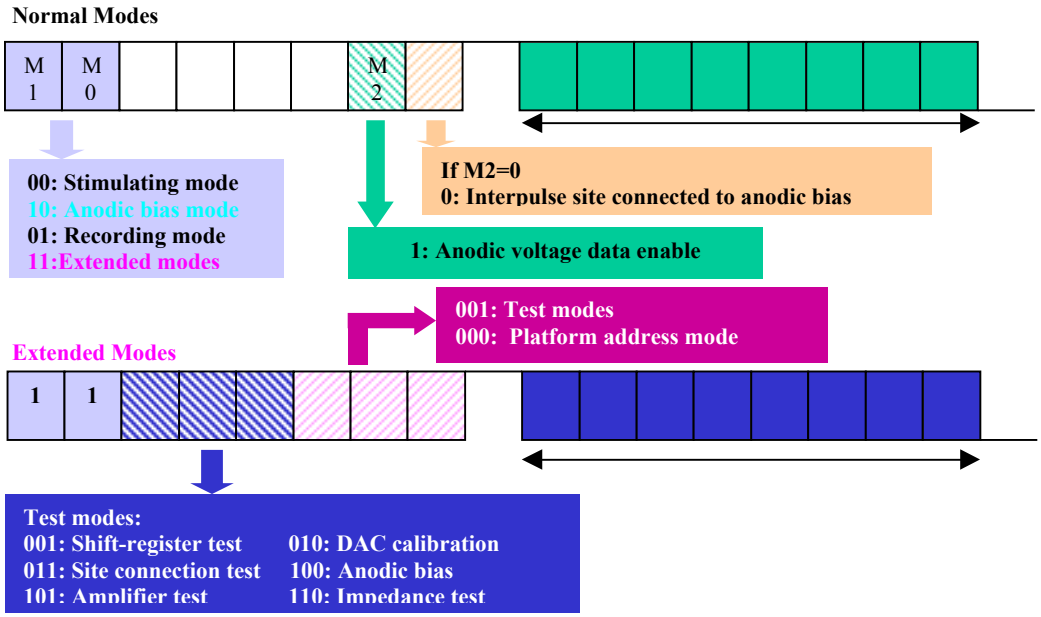
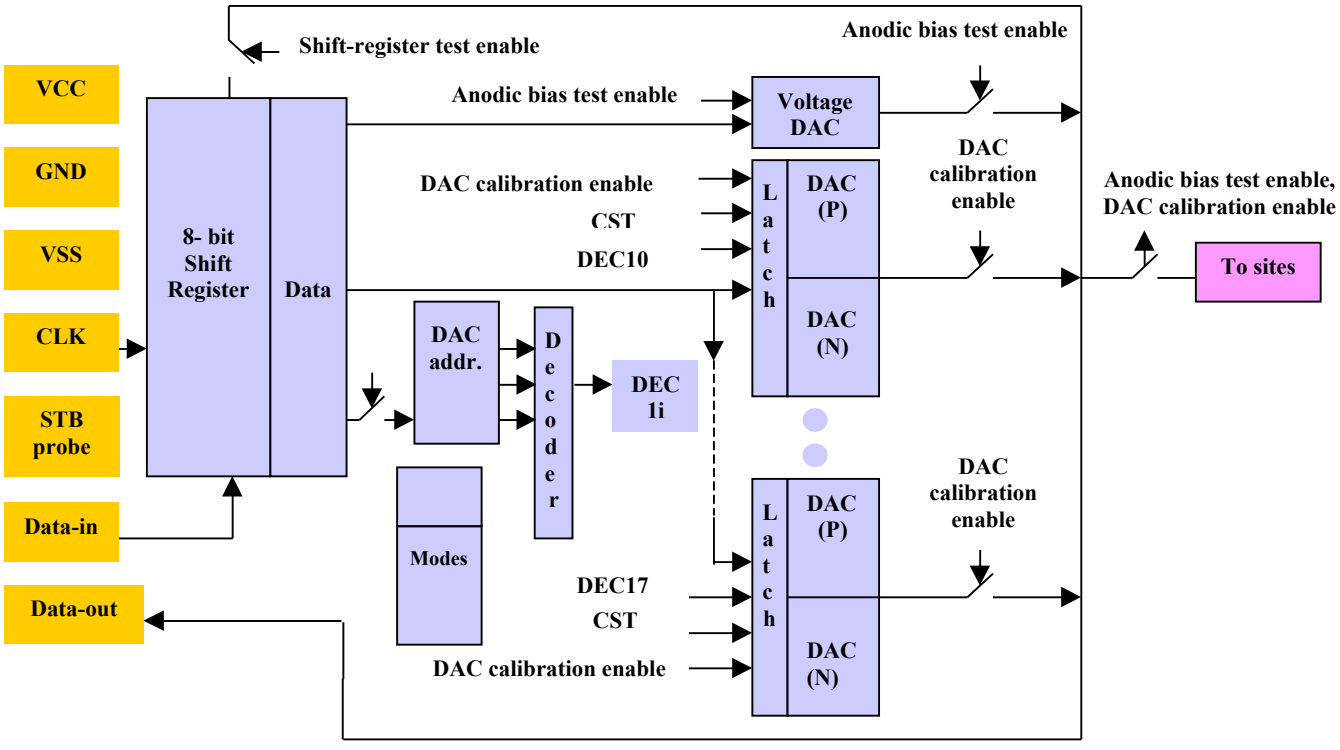
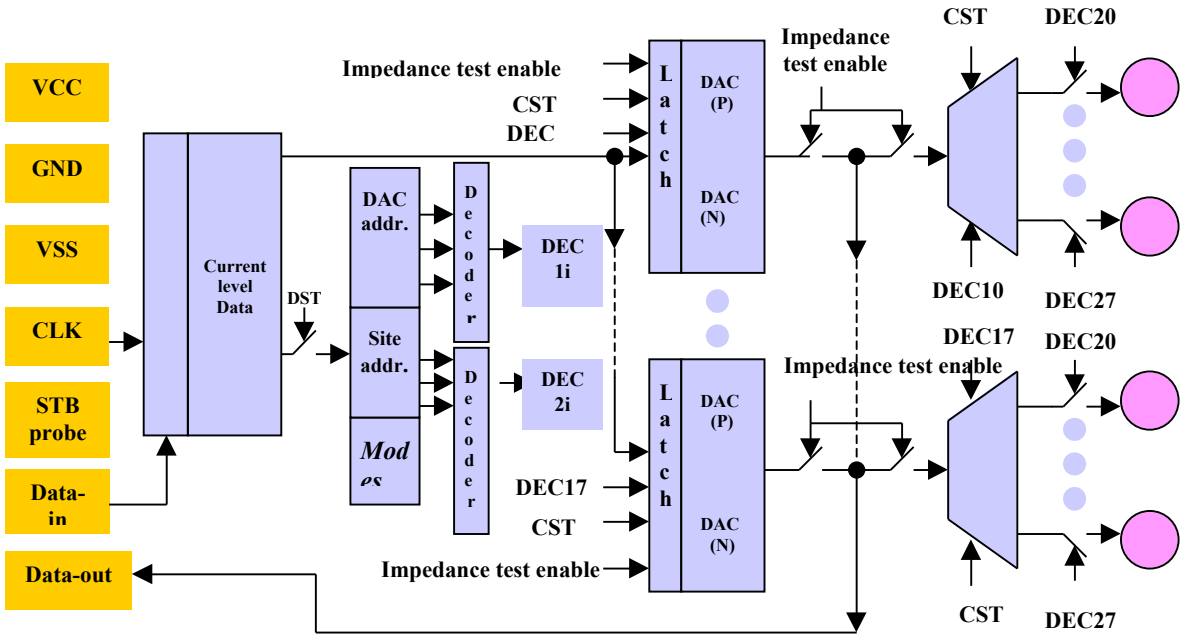


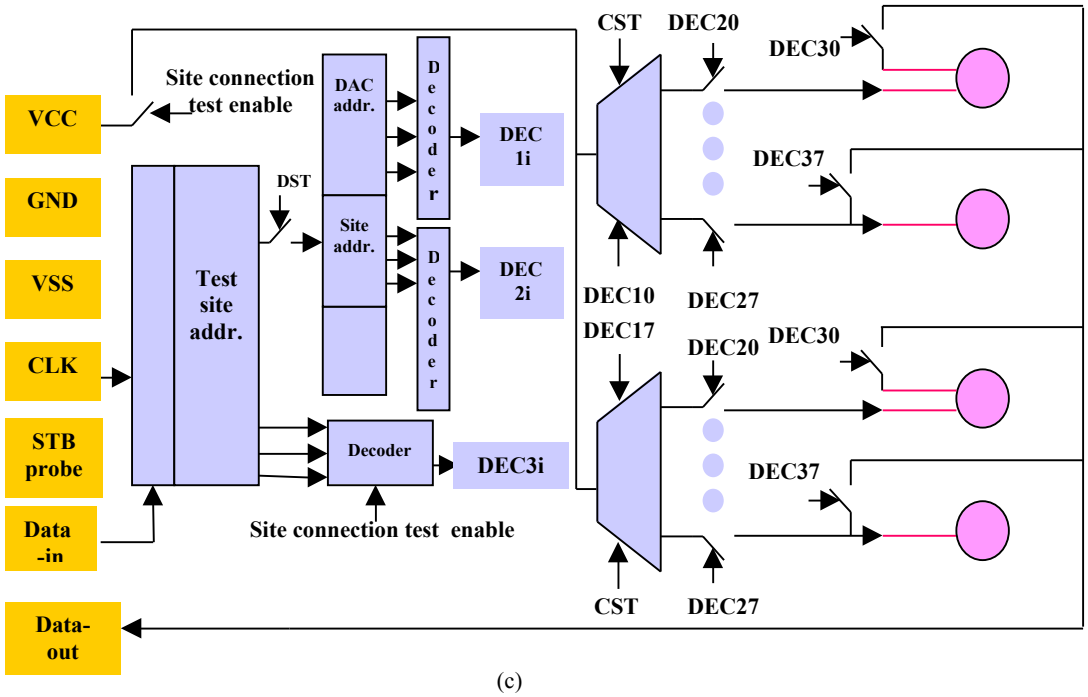
Fig. 3: Mode designations for STIM-2



(a)



(b)



(c)

Fig. 4: Block diagram for test modes: (a) shift register test, DAC calibration, and anodic bias test; (b) impedance test; and (c) site connection test.

As shown in Fig. 4(a), in the shift register test mode the serial output of the 8-bit shift register is directly connected to the output pad and the readout is compared with the clocked in data. In the DAC calibration or anodic bias test modes, the analog output of DAC or voltage source is connected to the output pad to see if the current or voltage level corresponds to the input digital data within a certain accuracy range. In Fig. 4(b) for the impedance test mode, both the DAC output and selected site are connected to the output pad. A certain current is delivered and the site voltage is monitored to obtain the site impedance. In Fig. 4(c) for site connection tests, the power supply is connected to the sites instead of the stimulating DAC. When one site is selected, all the 8 sites in the same channel are tested to check for any open or short circuits.

A new DAC design has also been developed using a high-swing cascode current source. SPICE simulations show improved output resistance, power supply independence and charge balance in the face of threshold voltage shifts. Figure 5 shows the simple current source used in the original STIM-2 DAC design, a conventional cascode current source, and the proposed high-swing cascode current source.

Cascode current sources have not previously been used in the stimulating probes because of their limited output swing. During current stimulation, the increased site voltage drop due to the charge transfer process tends to put the transistors out of saturation and rob the drive voltage of its ability to provide the desired current. For a $1000\mu m^2$ site area, we must limit the maximum stimulating current to around 100µA and use a relatively high supply voltage of 5V. Use of the stacked transistor configuration in a cascode current source will make the problem even worse. The diode connected T1/T2 (or T3/T4) makes the output swing nearly $V_t+2V_{ds,sat}$ below the +5V supply (or above –5V supply) as shown in Fig.5(b). The high-swing cascode current source uses Q1/Q2 to independently bias the stacked transistors T2, T3 as shown in Fig. 5(c) so that the output swing can be maximized to $2V_{ds,sat}$ below +5V or above –5V. Since the biasing current is very small in our application (~1µA), with relatively large transistors $V_{ds,sat}$ can be very small.

Figure 6 shows the output DC characteristics of the three designs. The solid line corresponds to the simple current design, the dashed line to the conventional cascode current source, and the dotted line to the high-swing cascode design. The output characteristic of the simple design is poor for a current source. The conventional cascode design has very high output resistance and the high-swing cascode design improves the linearity range by ~1V (we expect improvement of V_t from above analysis).

Figure 7 shows the power supply dependence of these designs. When the +5V supply (VCC) and the –5V supply (VSS) are changed by ±20%, the output currents vary almost linearly with the power supplies in all the designs. The high-swing cascode design gives relatively better power supply independence, but altogether since we use only simple bias circuitry, the power supply independence is not very good. This is not critical for a stimulating probe and in the original STIM-2 design, this supply dependence was used to calibrate the DACs. (When telemetry circuitry is integrated with the probe

circuitry, this might not be feasible.) Another important DAC specification is charge balance. Figure 8 shows the sourcing/sinking current variations with threshold shift.

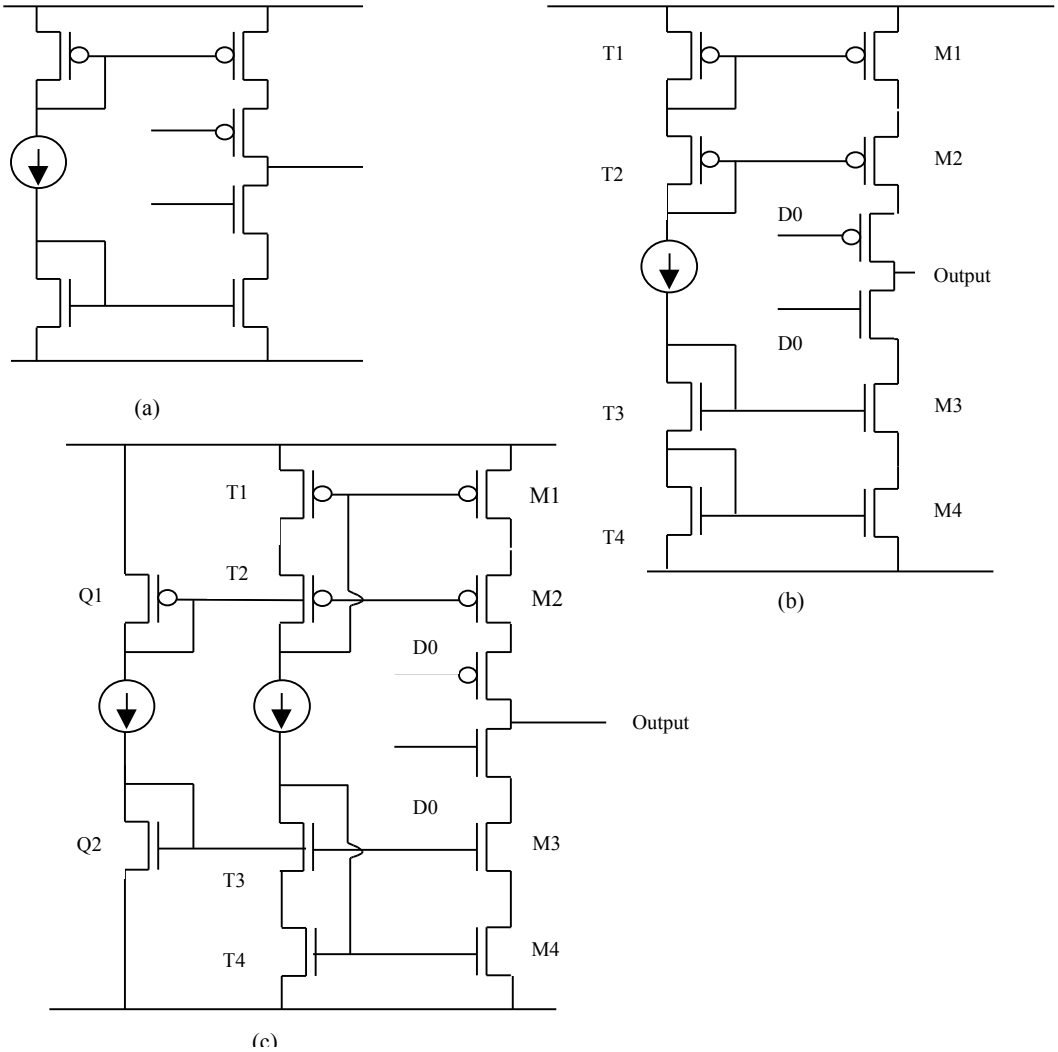


Fig. 5: A schematic of (a) a simple STIM-2 current source (b) a conventional cascode current source (c) the new high-swing cascode current source.

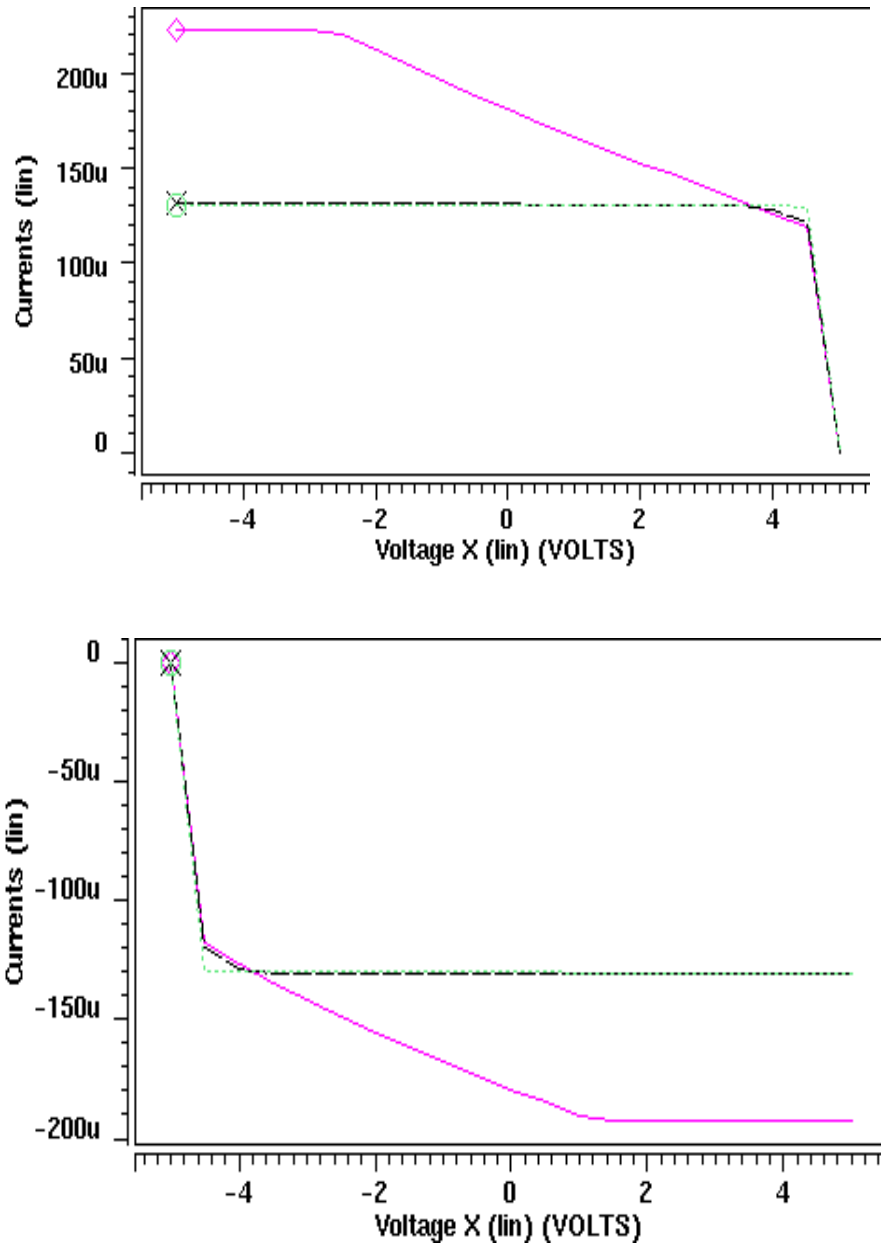


Fig. 6: (a) Output current vs. output voltage of the three designs while sourcing current; (b) Output current vs. output voltage of the three designs while sinking current

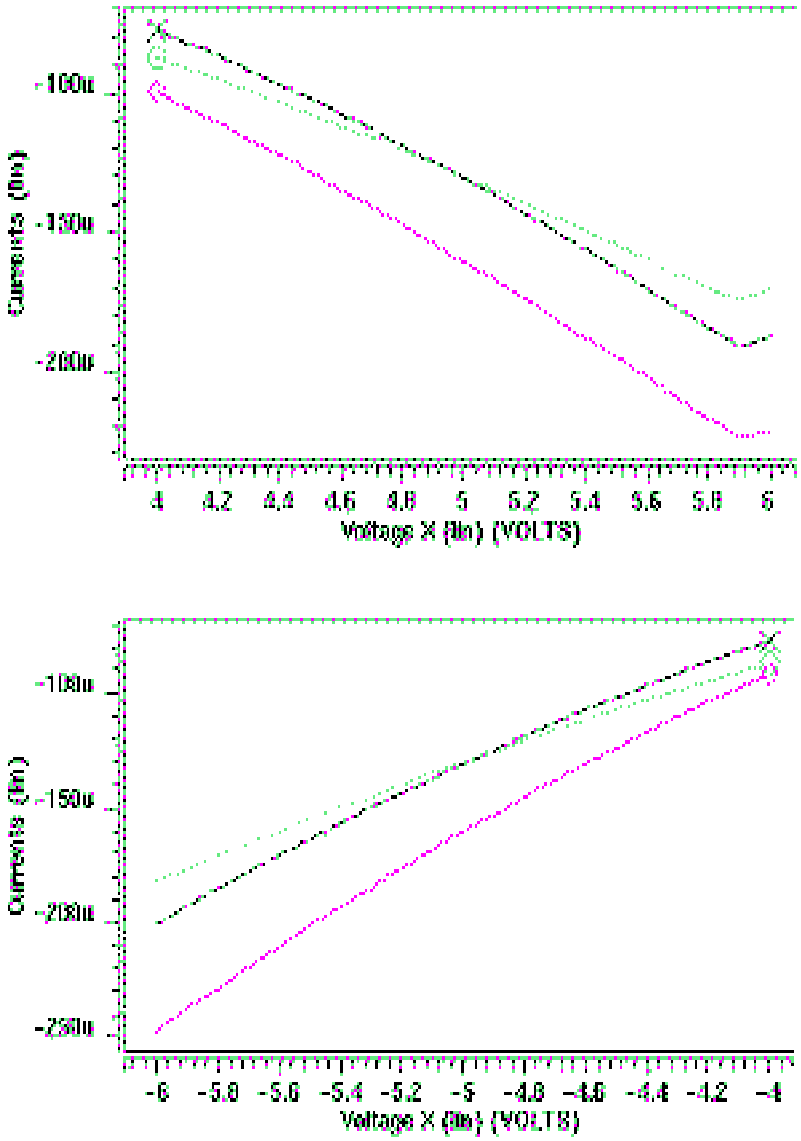


Fig. 7(a): Output current vs. Vcc (above), and (b) Output current vs. Vss (below). Again, the solid line represents the performance of the original STIM-2 DAC design, the dashed line is a conventional cascode, and the dotted line represents the new high-swing cascode design. While all three designs shows significant power-supply dependence, the new design is the best of the three.

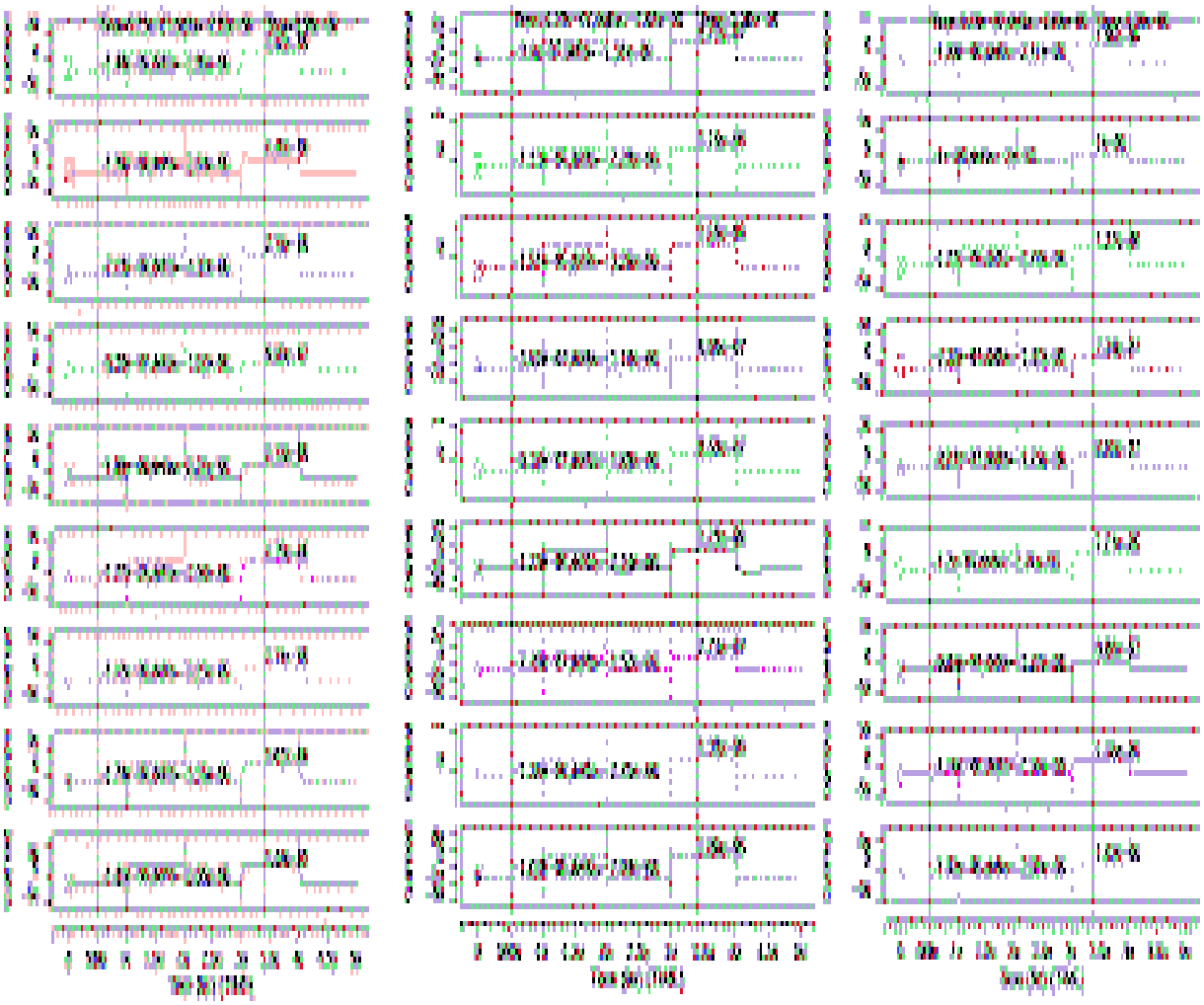


Fig. 8: Sourcing and sinking current vs. threshold voltage variation. From top, the threshold voltage is (Vt,nmos = 0.92V, Vt,pmos = -0.93V), (0.92V, -0.744V), (0.92V, -1.116V), (0.736V, -0.93V), (1.104V, -0.93V), (1.104V, -1.116V), (0.736V, -0.744V), (1.104V, -0.744V), (0.736V, -1.116).

The threshold voltages of the PMOS and NMOS transistors have been varied by ±20%. The high swing cascode design shows a very good charge balance (a maximum of 0.03µA variation for a 1µA stimulation current), which is very desirable in our application. A schematic of the high-swing DAC circuit with transistor sizes is shown in Fig. 9. Despite all the advantages discussed above, this design introduces additional bias branches and results in 10µW more of power dissipation for each channel, i.e., a total of 80µW more for 8 channels,. For a stimulating probe, this is probably not excessive.

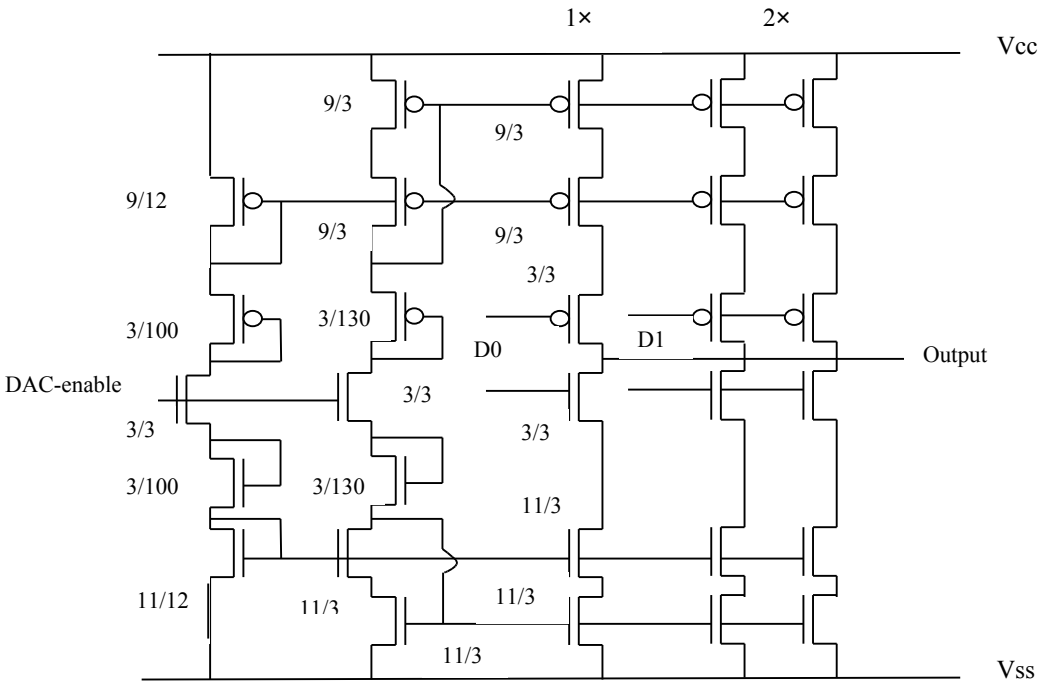


Fig. 9: A schematic of the high-swing cascode current source with transistor sizes.

3. A Telemetry-Powered CNS Stimulating System

The System Block Diagram:

In previous quarters the design and implementation of the power supply, clock generator, data detector and power-on reset was performed. During the last quarter, the timing controller and strobe generator block were designed and simulated. The functions of this block can be summarized as below and is shown in Fig. 10.

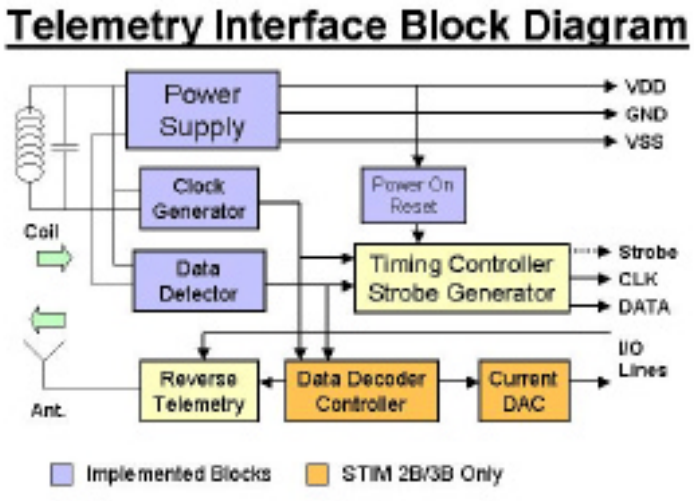


Fig. 10: Block diagram of the telemetry interface

1) This block receives the clock extracted from the carrier and steps it down with a user selectable ratio (N) to synchronize it with the demodulated data.
2) Temporarily stores the received data in a serial shift register and applies a parity check on every frame of 9 bits to eliminate false stimulation.
3) Generates strobe signals to synchronize STIM-2 with the interface chip and the external transmitter system.
4) Buffers the stepped down clock and demodulated data and sends it to the stimulating probe.

There is a minor difference between the original STIM-2 design and the new design. In the original design, to minimize the number of hard-wired interconnects, which were passing through the skin, strobe pulses were superimposed on the clock and data lines. To be distinguishable from data and clock pulses, these strobe pulses were negative going (3-level logic). However, in the new design, both the interface chip and the stimulating probe will be implanted, so there is less limitation in the number of interconnects between these two areas. Hence, the strobe signal is assigned a separate

line and is positive going like any other digital signal in the system. Controller block designs have been carried out for both methods to support all various conditions whether the number of interconnects is limited or not.

The Timing Controller and Strobe Generator Block Design:

One of the major limitations of the telemetry link versus hard-wired connection is the communication bandwidth. The original STIM-2, which was a hard-wire-connected stimulator, was designed to operate with a 4MHz clock frequency. The serial bit stream data rate could be as high as the clock frequency. But the wireless stimulating system is being designed based on a 4MHz carrier signal because of the tissue loss at higher frequencies. So the data baud-rate will be limited to about two orders of magnitude lower values to keep enough carrier cycles for a reliable amplitude demodulation and data detection scheme. This is one of the major limitations in interfacing with 3D-stimulating probes with large numbers of sites. To achieve higher data rates, the carrier frequency can be increased at the expense of higher tissue loss. But since in the present system design, the transmitter and receiver coils will be placed in close proximity and the tissue loss does not increase significantly for frequencies at tens of MHz, this should not cause a major problem.

Experimental measurements have shown that the maximum bit rate detected by the demodulator block is no more than 32kbit/sec, so the carrier frequency should be stepped down by a factor of 128. To be compatible with faster or slower demodulators based on process variations, a 9-bit counter slows down the input clock frequency in two stages of 5 and 4-bits. The reason for this 2-level frequency division is to give the user flexibility to choose a division factor of from 32 to 256 (32×N) with steps of 32 by cutting links on the fabricated chip. The default value for N is 15 with all four bits set high. A 4-bit comparator resets both counters whenever the value of the second stage counter equals N. A second comparator is used to generate an internal clock signal ($CK_{\%50}$) with 50% duty cycle and frequency of:

$$f_{\%50} = f_{carrier} / (32 \times N) \qquad (1)$$

As shown in Fig. 11, a 50% duty cycle clock is the best to discriminate between 1's and 0's in the pulse width modulated serial input bit stream, which is received from the envelope detector block. The transmitter sends 0's with a duty cycle less than 33% and 1's with a duty cycle more than 66%. The $CK_{\%50}$ rising edge shifts the stabilized D_{in} value into a 9-bit shift register, which stores one byte of data plus a parity bit. The shift register acts as a temporary storage for a byte-by-byte parity check (every 9 clock cycles) before sending them to the stimulator chip.

In case of any parity error detection, the internal reset signal activates and resets the entire shift register and counter values, so only a stream of zeros is sent to the stimulator chip, which does not lead to stimulation. Meanwhile the digital block synchronizes with the incoming data stream and receives the next data byte. This synchronization scheme can be activated intentionally at any time by sending a wrong

parity bit at the end of an arbitrary byte. The timing controller and strobe generator block diagram is shown in Fig. 12.

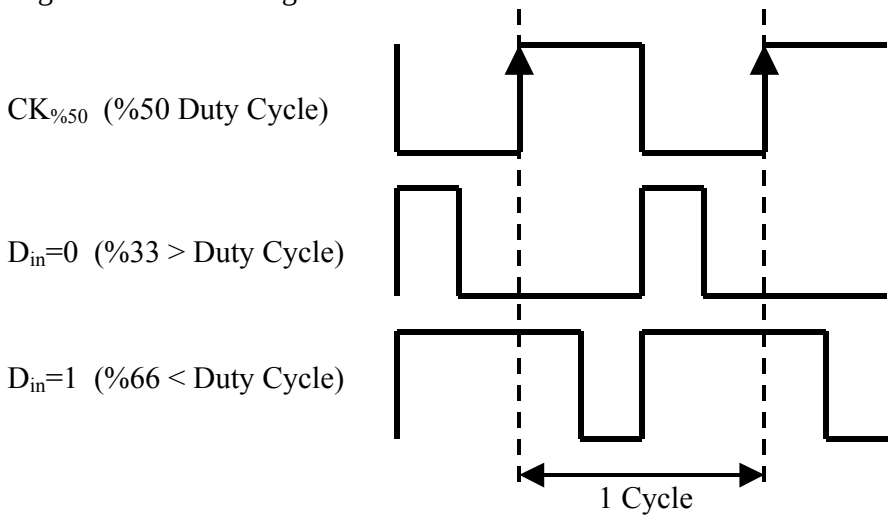


Fig. 11: The timing diagram of the internal clock and demodulated PWM data.

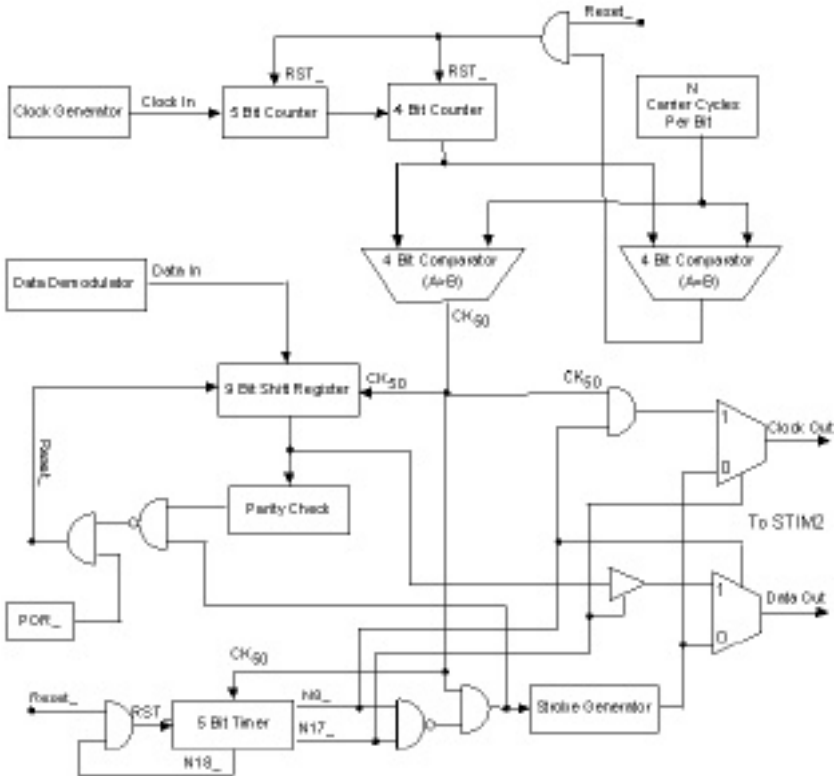


Fig. 12: The timing controller and strobe generator block diagram.

The clock and data input timing diagram of the STIM-2 is shown in Fig. 13. To keep the telemetry interface chip and STIM-2 synchronized, negative going strobe pulses should be added to clock (CK_{out}) and data (D_{out}) signals alternatively after each byte. So each of these signals has one negative half-cycle strobe pulse every 18 clock cycles. This is controlled by a 5-bit counter, which generates N8, N17 and N18 signals while receiving 9^{th}, 18^{th} and 19^{th} clock cycle respectively. 2 to 1 multiplexers at digital block outputs connect D_{out} and CK_{out} lines to the strobe generator and zero respectively at 9^{th} clock. At 18^{th} clock demultiplexers connect CK_{out} to the strobe generator while making D_{out} high impedance for the STIM2 to transmit any acquired signal back.

Figures 14(a) and (b) show the circuit schematics of the combined output demultiplexer, buffer and strobe generator of the clock and data output lines, respectively. These 3-level logic circuits can transfer clock and data pulses while buffering them as well as switching to the negative strobe pulses at proper timing between the frames. The strobe generator is a CMOS level shifter, which can convert standard input logic signals (V_{cc}(H) and GND(L)) to strobe output pulses (V_{cc}(H) and V_{ss}(L)). This part of the circuit is connected between V_{cc} and V_{ss} and has no static power consumption. But it can pass large transient currents while switching if proper NMOS-PMOS transistor sizing is not followed. To minimize transient current, the upper PMOS transistors should be much stronger than the lower NMOS cross-coupled pair. Both data, clock and strobe signals are buffered through successive scaled inverters to be strong enough to drive large interconnect ribbon cable capacitive loads (modeled by the output capacitors). Here, there is a difference between the clock and data line drivers. The former is always driving the clock line while the latter has a tri-state output buffer which can disconnect the data line from the interconnect bus during the 18^{th} clock cycle for the STIM2 reverse data transmission. The last stage is a 2-to-1 demultiplexer, which chooses between the input (data or clock) and the strobe signal based on the *str* input, which is generated by the timer block. Figure 15 shows simulation results of this part of the circuit, which successfully resembles the timing diagram of the STIM2 in Fig. 13.

As mentioned above, the new STIM-2 design uses a separate strobe line with positive pulses. Figure 16 shows the new timing diagram.

The timing controller and strobe generator design were changed accordingly to stay compatible with the new design. Figure 17 shows a part of the controller which generates the data, clock and strobe signals. The strobe output is separated from data and clock outputs and it is a normal positive pulse. Each command in the normal mode consists of two frames. The first and the second frames are discriminated by forcing *Data=High* and *Clock=Low* at the 9^{th} clock cycle (by the end of the first frame), and *Data=Low* and *Clock=high* at the 18^{th} clock cycle (by the end of the second frame). Figure 18 shows the simulation results of the circuit of Fig. 17 and resembles the timing scheme shown in Fig. 16.

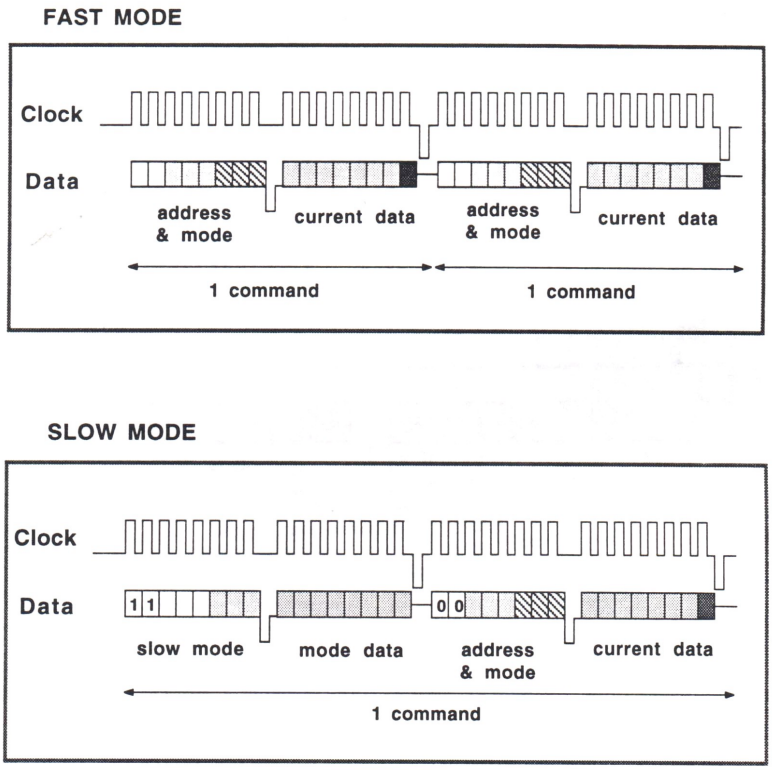
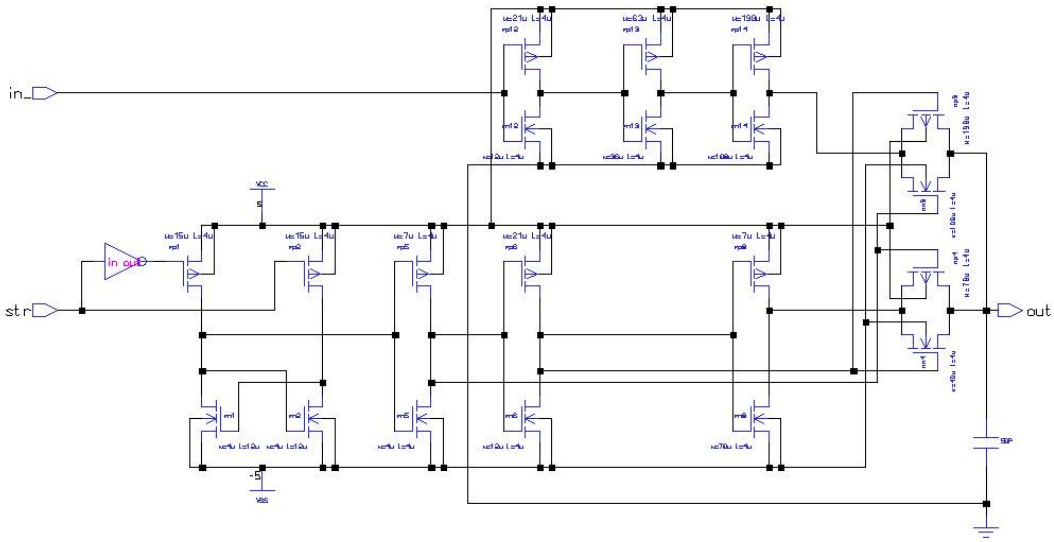
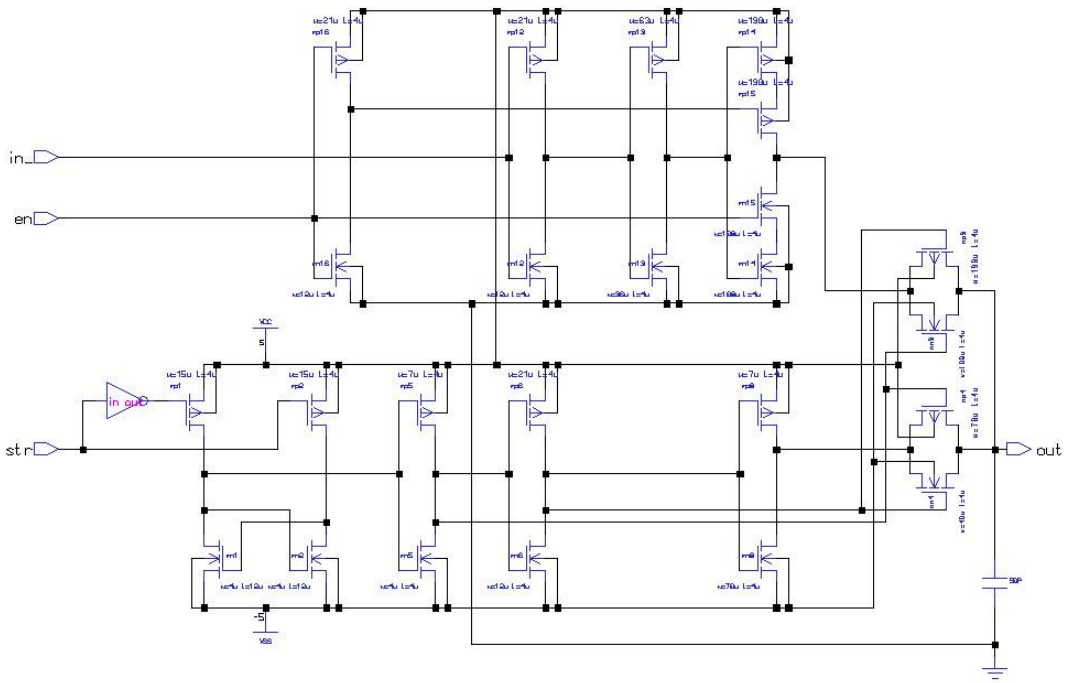


Fig. 13: The timing diagram of the first STIM-2 design.



(a)

Fig. 14(a): Clock circuit.



(b)

Fig. 14(b): Data strobe generator, demultiplexer, and buffer circuits

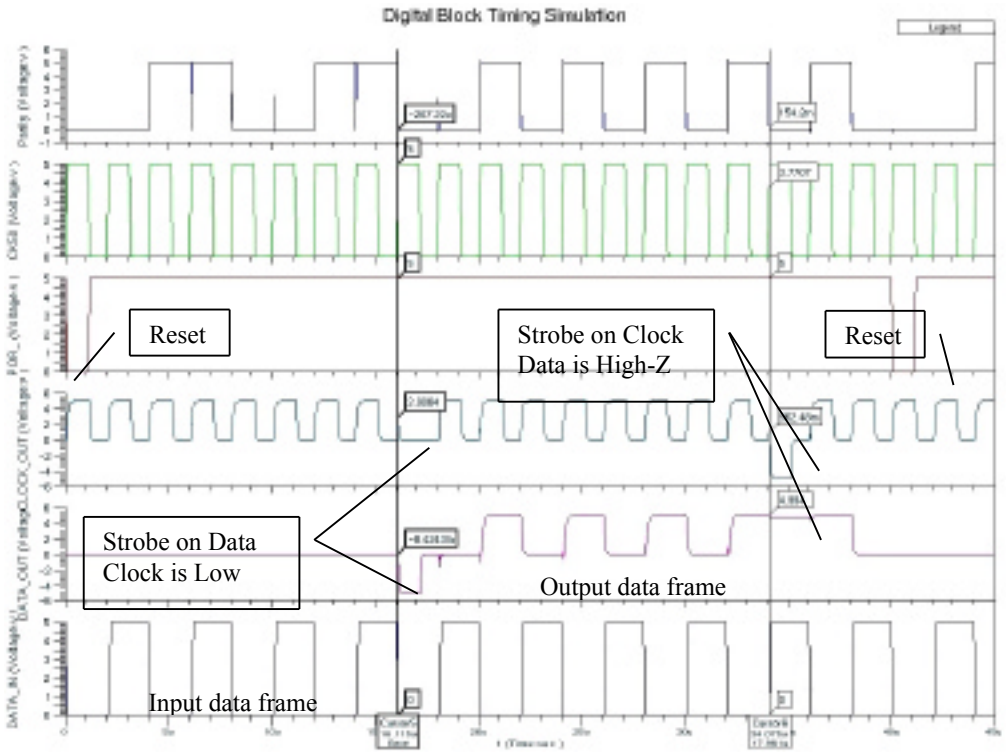


Fig. 15: Simulation waveforms of the timing controller and strobe generator block.

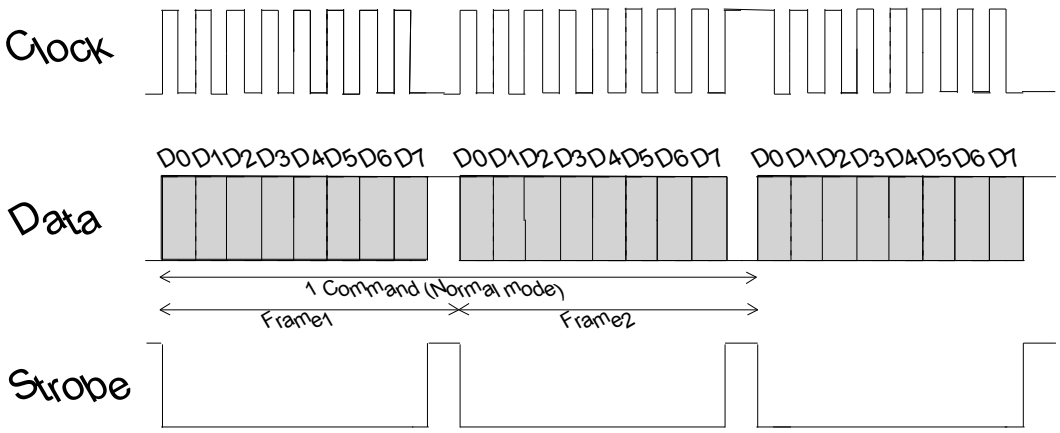


Fig. 16: The new STIM-2 timing diagram.

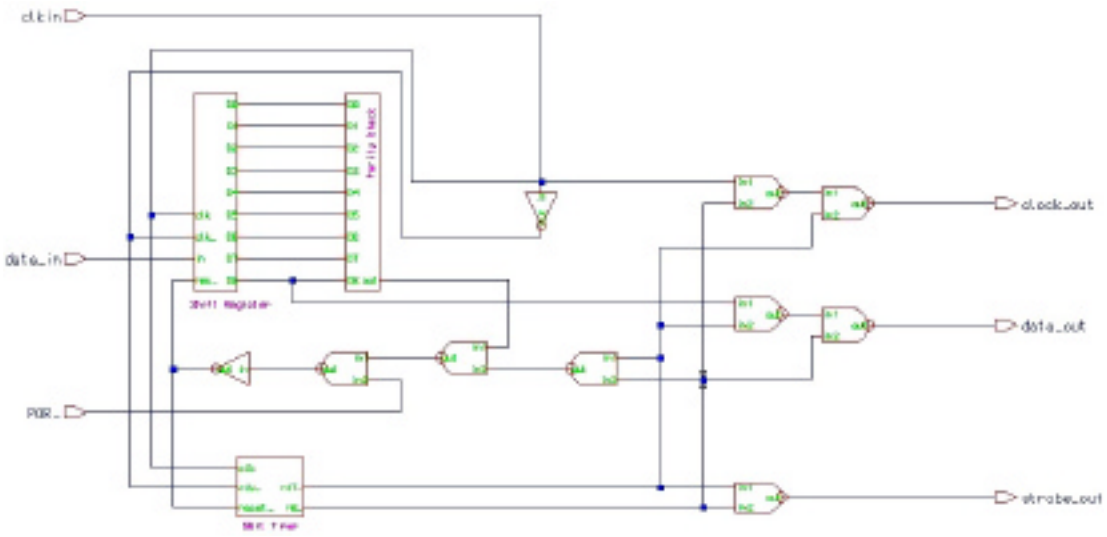


Fig. 17: The new timing controller and strobe generator design.

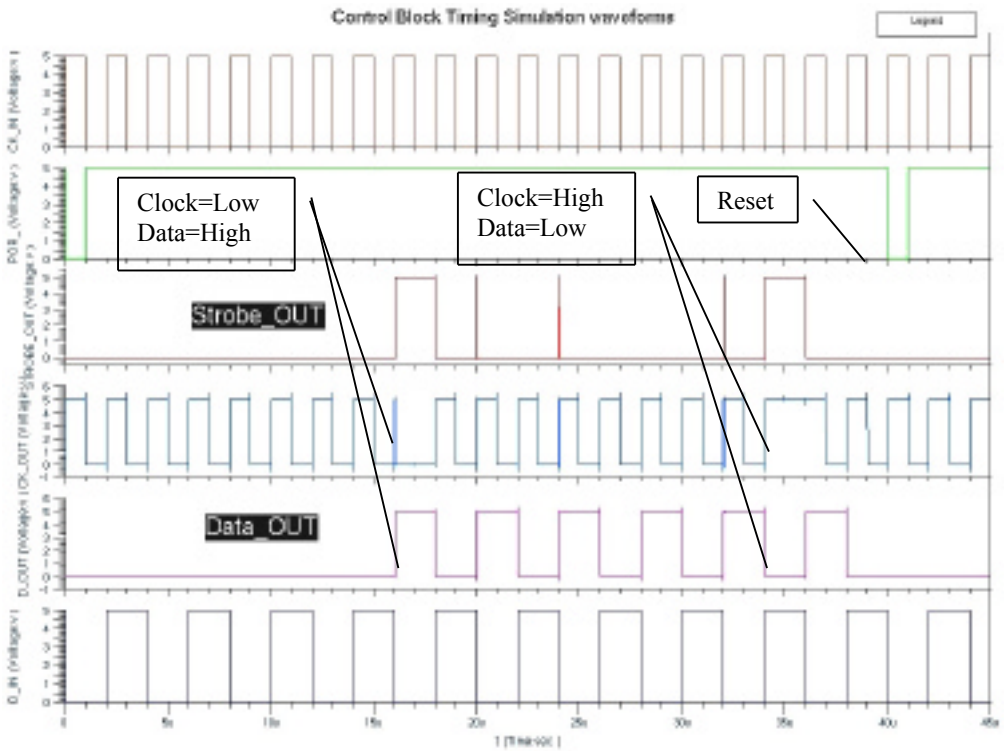


Fig. 18: Simulation results of the new timing controller and strobe generator block.

4. Conclusions

During the past quarter, with the completion of STIM-2B/-3B, we have shifted more focus to completing the redesign of STIM-2/-3 and to the development of the telemetry circuits that will be needed to make these probes operate wirelessly via a telemetry interface. The negative strobes needed for the original STIM-2 design have been replaced so the interface requires only 5V logic. Separate address and data latching signals are generated on-chip by holding the CLOCK and DATA lines at designated levels during the strobe, effectively providing masking capability. In 3D probe assemblies, the strobe signal is decoded in platform electronics and is gated to only the addressed probe so that the others perform no operation when they are not addressed.

A major problem with present active probes, and especially stimulating probes, is the difficulty associated with testing the devices before final bonding and use. This is particularly true of 3D arrays where it is critical to assemble only known good devices into the arrays. At present, sites must be probed individually, requiring hours to verify the operation of each probe prior to final assembly. Test modes have been added to the redesigned STIM-2/-3 probes to allow complete testing of the probes before the final release etch and after this etch but before bonding/assembly. The test modes include: input shift register test, DAC calibration, site connection test, anodic bias test, amplifier test, and site impedance test. Thus, all important aspects of the probes can be tested from

the normal probe I/O connections. This applies not only to pre-assembly but also to tests performed in-vitro and in-vivo.

A new DAC design has also been developed for STIM-2/-3 that offers much improved output resistance, power-supply independence, and charge balance in the face of device threshold variations.

In developing the circuitry required for a fully-implantable wireless interface to the probes, we have previously reported the development of the power supply, clock generator, data detector, and power-on-reset circuits. During this last quarter, the timing controller and strobe generator circuits were designed and simulated. This block receives the clock and steps it down with a user selectable ratio to synchronize it with the demodulated input data. The data is stored in a serial shift register and parity checks are performed. Strobe signals are generated to synchronize the data to STIM-2 and the clock and data is sent to the stimulating probe. We hope to have the full telemetry interface for the stimulating probes designed, integrated, and tested before the end of the year.